Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. -7. (Cancelled).

8. (Currently Amended) A method of manufacturing a mask read only memory, comprising sequential steps of:

providing a semiconductor structure having a first opening therein;

forming a first glue layer on a surface of said semiconductor structure extending into said first opening;

forming a contact plug within said first opening in said semiconductor structure, said contact plug ~~comprises~~ comprising a first glue layer lining said first opening and a first metal layer in said first opening ~~therein and a first glue layer thereon~~;

etching said first glue layer outside said contact plug in order to expose said surface of said semiconductor structure;

forming a patterned photoresist layer on said semiconductor structure;

forming a plurality of code areas in said semiconductor structure by using said patterned photoresist layer as a mask;

removing said patterned photoresist layer; and

forming a second glue layer on said semiconductor structure.

9. (Currently Amended) The method of claim 8, wherein said semiconductor structure comprises a plurality of buried bit lines therein ~~and a first dielectric layer thereon~~.

10. (Original) The method of claim 9, wherein each of said plurality of code areas is formed between two of said buried bit lines.

11. (Original) The method of claim 8, wherein said first metal layer is deposited to cover said first glue layer.

12. (Original) The method of claim 11, wherein said contact plug is formed by planarizing said first metal layer.

13. (Original) The method of claim 8, wherein the material of said first metal layer is tungsten.

14. (Original) The method of claim 8, wherein said etching said first glue layer outside said contact plug in order to expose said surface of said semiconductor structure comprises a blanket etching back process.

15. (Original) The method of claim 8, wherein said forming said plurality of code areas in said semiconductor structure by using an ion implantation process.

16. (Cancelled).

17. (Original) The method of claim 8, wherein the material of said first glue layer is titanium/titanium nitride (Ti/TiN).

18. (Original) The method of claim 8, wherein said second glue layer comprises linear

titanium/titanium nitride (Ti/TiN).

19.-23. (Cancelled).

24. (New) The method of claim 8, wherein said semiconductor structure comprises a dielectric layer on top thereof.

25. (New) The method of claim 24, wherein the material of said dielectric layer comprises Borophosphosilicate Glass (BPSG).

26. (New) The method of claim 24, wherein said dielectric layer comprises a first dielectric layer and a second dielectric on said first dielectric layer.

27. (New) The method of claim 26, wherein said first opening is formed in said second dielectric of said semiconductor structure.

28. (New) The method of claim 26, wherein said second dielectric is Borophosphosilicate Glass (BPSG).

29. (New) The method of claim 8, wherein said patterned photoresist layer comprises a second opening corresponding to an area between two of said plurality of buried bit lines.